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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,442	04/20/2004	Katsuya Arai	60188-841	2727

7590 04/18/2007

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	PAPER NUMBER
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/827,442	ARAI ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/23/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6 and 10-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 11-16* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☒ Claim(s) *6, 10,17* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 11, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Patent No. 6,920,026, in view of Voldman, Patent No. 6,455,902.

With respect to claim 1, Chen discloses a semiconductor integrated circuit device [Fig. 8] comprising an external connection terminal [Fig. 8, 120]; an electrostatic discharge protection circuit [Fig. 8, consists of Mp51, Mn51] connected to the external connection terminal; a power supply line [Fig. 8, VDD] connected to the electrostatic discharge protection circuit; a ground line [Fig. 8, VSS] connected to the electrostatic discharge protection circuit; and an inter-power supply electrostatic discharge protection circuit [Fig. 8, 15] that is connected to the power supply line [Fig. 8, VDD] and the ground line [Fig. 8, VSS], and has a gate insulating element [Fig. 8, transistor Mn8], wherein the inter-power supply electrostatic discharge protection circuit comprises a first gate voltage circuit [Fig. 8, consists of capacitor C6 and resistor R7] capable of controlling the gate voltage of the gate insulating element [Fig. 8, transistor Mn8] as disclosed in Col. 12, lines 31 – Col. 13, lines 20]; the gate insulating element

[Fig. 8, Mn8] is a first NMOS transistor whose source is connected to the ground line [Fig. 8, VSS] and whose drain is connected to the power supply line [Fig. 8, VDD]. Chen does not disclose that the gate-insulating element is a first NMIS transistor. However, use of one conductivity-type transistor over a complementary conductivity-type transistor, whether one replaces a transistor with the other or complements the overall circuit with the other transistor would have been obvious and well within the abilities of one having ordinary skill in the art. However, Chen does not disclose that the first gate voltage control circuit comprises a first Schmidt trigger circuit, and a specific resistor and capacitor arrangement.

Voldman discloses an ESD protection circuit for semiconductor chips. Voldman discloses that the first gate voltage control circuit [Fig. 7, consists of 72 and 80] comprises a first Schmidt trigger circuit [Fig. 7, inverters 80] connected at its output to the gate of the first NMOS transistor [Fig. 7, 70]; a resistor [Fig. 7, resistor in 72] whose one end is connected to the power supply line [Fig. 7, V1] and whose other end is connected to an input of the first Schmidt trigger circuit [Fig. 7, inverters 80]; and a capacitor [Fig. 7, capacitor in 72] whose one end is connected to the ground line [Fig. 7, V2] and whose other end is connected to the input of the first Schmidt trigger circuit [Fig. 7, inverters 80].

Chen and Voldman both disclose RC coupled electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Voldman's first gate voltage

circuit with Chen's ESD circuit, in order to incorporate the use of inverters/Schmidt triggers devices as it allows for a fast-setting response time for the RC circuit without worrying about the Vdd-Vss shunting device from shunting-off too quickly.

With respect to claim 11, Chen discloses that the device comprises an input buffer circuit [Fig. 11, Pre-buffer] connected to the external connection terminal [Fig. 11, 140].

With respect to claim 14, Chen discloses that the device further comprises an internal circuit [Fig. 8, 1] connected to the external connection terminal [Fig. 8, 120].

With respect to claim 15, Chen discloses that the electrostatic discharge protection circuit [Fig. 10] comprises a fist PMOS transistor [Fig. 10, Mp62] whose source is connected to the power supply line [Fig. 10, VDD], whose drain is connected to the external connection terminal [Fig. 10, 130], and whose n-type substrate region is connected to the power supply line; and a third NMOS transistor [Fig. 10, Mn62] whose source is connected to ground line [Fig. 10, VSS], whose drain is connected to the external connection terminal [Fig. 10, 130], and whose p-type substrate region is connection to the ground line {fig. 10, VSS].

With respect to claim 16, Chen discloses that the device further comprises a resistor [Fig. 10, R12] interposed between the gate of the third PMOS transistor [Fig. 10, Mp62] and the power supply line [Fig. 1, VDD]; and a resistor [Fig. 10,

R11] interposed between the gate of the third NMOS transistor [Fig. 10, Mn62] and the ground line [Fig. 10, VSS].

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of Voldman, Patent No. 6,455,902.as applied to claim1 above, and further in view of Ker et al., Patent No. 6,437,407.

With respect to claim 12, Ker teaches that the integrated circuit further comprises an output circuit [Fig. 7, consists of transistors 704 and 704'] connected to the external connection terminal [Fig. 7, 702]; and an output pre-buffer circuit [Fig. 7, consists of transistors 708, 710, 708', 710'] connected to the output circuit.

Chen, Voldman, and Ker are analogous electrostatic discharge protection circuits for integrated circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Ker's output circuit and an output pre-buffer circuit, with Chen's ESD circuit, because the ESD clamp device is disposed on an output buffer in order to clamp the ESD overstress voltage across the gate oxide during an ESD event.

With respect to claim 13, Ker teaches that the output pre-buffer circuit comprises a first pre-buffer circuit [Fig. 7, consists of transistors 708 and 710] having at its last stage a first pre-buffer connected to the power supply line [Fig. 7, VDD], and a second pre-buffer circuit [Fig. 7, consists of transistors 708' and 710'] having at its last stage a second pre-buffer connected to the power supply line [Fig. 7, VDD], and wherein the output circuit comprises a second PMOS

transistor [Fig. 7, 704] whose source is connected to the power supply line [Fig. 7, VDD], whose drain is connected to the external connection terminal [Fig. 7, 702], whose gate is connected to an output terminal of the first pre-buffer, and whose n-type substrate region [Fig. 7, substrate terminal of PMOS transistor 704] is connected to the power supply line [Fig. 7, VDD]; and a second NMOS transistor [Fig. 7, 704'; The PMOS transistor 704' can be replaced by an NMOS transistor, because the drains and sources are fully interchangeable in MOSFETS].whose source is connected to the ground line [Fig. 7, VSS], whose drain is connected to the external connection terminal [Fig. 7, 702], whose gate is connected to an output terminal of the second pre-buffer and whose p-type substrate region [Fig. 7, substrate terminal of NMOS transistor 704'] is connected to the ground line [Fig. 7, VSS].

Allowable Subject Matter

Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 18: The prior art discloses a first inverter section that is connected at its input to the other end of the resistor and the other end of the capacitor; a second inverter section that is connected at its input to the output of the first inverter section; a third inverter section that is connected at its input to the output of the second inverter section and is connected at its output to the

gate of the first NMOS transistor; but does not disclose a further inverter section that is connected at its input to the output of the second inverter section and is connected at its output to the input of the second inverter sections. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Response to Arguments

Applicant's arguments filed 01/23/2007 have been fully considered but they are not persuasive.

Applicant comments on page 7 of the remarks that Chen does not disclose or even suggest the use of a Schmidt trigger circuit, and the arrangement of the capacitor and resistor as taught by Chen is opposite.

A new reference by Voldman [Patent No. 6,455,902] discloses the use of a Schmidt trigger device/inverters as recited in amended claim 1, and the correct arrangement of the capacitor and resistor as claimed.

Applicant comments on pages 7-8 of the remarks regarding the Wu reference. However, this reference has been removed from the above rejection, and a new reference by Voldman has been used.

Based on examiner's best understanding, it is believed that the prior art reference by Chen and Voldman read on the amended claim language of independent claim 1.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DHP
04/10/2007

Stephen W Jackson

4-11-07

STEPHEN W. JACKSON
PRIMARY EXAMINER